

WHAT IS CLAIMED IS:

- 1 1. A method of manufacturing a semiconductor device, comprising:
 - 2 forming a gate oxide over a substrate and a gate electrode over the gate oxide;
 - 3 implanting impurities into the substrate using the gate electrode as an implant
 - 4 mask to form a lightly-doped region in the substrate;
 - 5 depositing second spacer material adjacent the gate electrode;
 - 6 forming a first spacer on the second spacer material;
 - 7 implanting impurities into the substrate and through a portion of the lightly-doped
 - 8 region using the first spacer as an implant mask to form a first junction region in the
 - 9 substrate;
 - 10 removing the first spacer;
 - 11 etching the second spacer material to form a second spacer adjacent the gate
 - 12 electrode; and
 - 13 implanting impurities into the substrate using the second spacer as an implant
 - 14 mask to form a second junction region in the substrate.
- 1 2. The method of Claim 1, further including depositing additional second spacer
 - 2 material on the initially deposited second spacer material prior to etching the second
 - 3 spacer material.
- 1 3. The method of Claim 1, wherein said first junction region is a deep junction
 - 2 region and said second junction region is a source/drain region.

- 1 4. The method of Claim 1, wherein said first spacer comprises an oxide, and said
2 second spacer material comprises a nitride.
- 1 5. The method of Claim 1, wherein the second spacer has a width less than a width
2 of the first spacer.
- 1 6. The method of Claim 3, further including forming a silicide over the source/drain
2 region.
- 1 7. The method of Claim 1, wherein the substrate is a silicon-on-insulator substrate.
- 1 8. The method of Claim 1, wherein the lightly-doped region has a dopant
2 concentration in the range of about $1 \times 10^{18} \text{cm}^{-3}$ to about $1 \times 10^{20} \text{cm}^{-3}$.
- 1 9. The method of Claim 1, wherein the first junction region has a dopant
2 concentration in the range of about $1 \times 10^{17} \text{cm}^{-3}$ to about $1 \times 10^{20} \text{cm}^{-3}$.
- 1 10. The method of Claim 1, wherein the second junction region has a dopant
2 concentration in the range of about $1 \times 10^{18} \text{cm}^{-3}$ to about $1 \times 10^{21} \text{cm}^{-3}$.

1 11. A method of manufacturing a short channel semiconductor device, comprising:
2 forming a gate oxide over a substrate and a gate electrode having a gate width of
3 less than 0.13 micron over the gate oxide;
4 implanting impurities into select regions of the substrate using the gate electrode
5 as an implant mask to form a lightly-doped region in the substrate having a channel
6 region extending therebetween beneath the gate oxide, the channel region having a
7 channel length of less than 0.13 micron;
8 depositing a bottom layer over the gate electrode and the substrate, and an upper
9 layer over the bottom layer;
10 removing portions of the upper layer to form a first spacer adjacent the gate
11 electrode;
12 implanting impurities through a portion of the lightly doped region using the first
13 spacer as an implant mask to form a first junction region in the substrate;
14 removing the first spacer;
15 removing portions of the bottom layer to form a second spacer adjacent the gate
16 electrode; and
17 implanting impurities through a portion of the lightly doped region and into the
18 substrate using the second spacer as an implant mask to form a second junction region in
19 the substrate.

1 12. The method of Claim 11, further including depositing additional bottom layer
2 material on the initially deposited bottom layer prior to removing portions of the bottom
3 layer to form the second spacer.

- 1 13. The method of Claim 11, wherein said first junction region is a deep junction
2 region and said second junction region is a source/drain region.
- 1 14. The method of Claim 11, wherein depositing an upper layer comprises depositing
2 an upper layer comprising an oxide, and wherein depositing a bottom layer comprises
3 depositing a bottom layer comprising a nitride.
- 1 15. The method of Claim 11, wherein removing portions of the bottom layer to form a
2 second spacer further comprises removing portions of the bottom layer to form a second
3 spacer having a width less than a width of the first spacer.
- 1 16. The method of Claim 11, further including forming a silicide over the second
2 junction region.
- 1 17. The method of Claim 11, wherein the substrate is a silicon-on-insulator substrate.
- 1 18. The method of Claim 11, further including:
2 forming a dielectric over the gate electrode and the second junction region;
3 forming a contact opening through said dielectric; and
4 forming an interconnect in said contact opening, the interconnect being
5 electrically coupled to said second junction region.
- 1 19. The method of Claim 11, wherein removing the first spacer comprises performing
2 an etch step using hot H₃PO₄ acid.

- 1 20. The method of Claim 11 further comprising forming a liner layer on the gate
- 2 electrode and the substrate prior to depositing the bottom layer.

1 21. A semiconductor device comprising:
2 a gate structure formed over a semiconductor region;
3 a lightly doped source/drain region formed in the semiconductor region to a first
4 depth, the lightly doped source/drain region substantially aligned with a sidewall of the
5 gate structure;
6 a sidewall spacer formed along a sidewall of the gate structure;
7 a heavily doped source/drain region formed in the semiconductor region to a
8 second depth deeper than the first depth, the heavily doped source/drain region
9 substantially aligned with an outer edge of the sidewall spacer; and
10 a deep source/drain region formed in the semiconductor region to a third depth
11 deeper than the second depth, the deep source/drain region spaced a lateral distance from
12 the outer edge of the sidewall spacer.

1 22. The device of claim 21 and further comprising:
2 a second sidewall spacer formed along a second sidewall of the gate structure;
3 a second lightly doped source/drain region formed in the semiconductor region to
4 the first depth, the second lightly doped source/drain region substantially aligned with a
5 second sidewall of the gate structure;
6 a second heavily doped source/drain region formed in the semiconductor region to
7 the second depth, the second heavily doped source/drain region substantially aligned with
8 an outer edge of the second sidewall spacer; and
9 a second deep source/drain region formed in the semiconductor region to the third
10 depth, the second deep source/drain region spaced a lateral distance from the outer edge
11 of the second sidewall spacer.

1 23. The device of claim 21 wherein the lightly doped source/drain region, the heavily
2 doped source/drain region, and the deep source/drain region are formed from impurities
3 of the same conductivity type.

1 24. The device of claim 23 wherein the lightly doped source/drain region, the heavily
2 doped source/drain region, and the deep source/drain region are formed from impurities
3 of the same material.

1 25. The device of claim 21, further comprising a silicide region formed at the surface
2 of the semiconductor region adjacent the outer edge of the sidewall spacer.